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Design of Memory Cell for Low Power Applications

N.geetha Rani*, DR.P.Chandrasekhar Reddy**
* Associate Professor, ECE Department, Ravindra College of Engineering for Women, Kurnool, A.P
** Professor, ECE Department, JNTUH College of Engineering, Hyderabad, A.P

ABSTRACT
Aggressive CMOS scaling results in lower threshold voltage and thin oxide thickness for transistors manufactured in nano regime. As a result, reducing the sub-threshold and tunneling gate leakage currents has become crucial in the design of ICs. This paper presents a new method to reduce the total leakage power dissipation of static random access memories (SRAMs) while maintaining their performance.
***Keywords* -** Leakage currents, SRAM, power consumption

I. INTRODUCTION

With diminishing process feature sizes and operating voltages, the control of leakage currents in modern VLSI designs is becoming a significant challenge. Leakage currents increase exponentially with decreasing threshold voltages. The power consumed by a design in the standby mode of operation is due to leakage currents in its devices. With the prevalence of portable electronics, it is crucial to keep the leakage currents of a design small in order to ensure a long battery life in the standby mode of operation. The leakage current for a PMOS or NMOS device corresponds to the $I_{ds}$of the device when the device is in the cutoff or sub-threshold region of operation. The expression for this current [2] is

$$I_{ds}=W/L\ I_o e^{(Vgs-VT-Voff/\eta Vt)}\ (1-e^{(-Vds/Vt)}) \quad (1)$$

Here I_o and V_{off} (typically V_{off} = -.08V) are constants, while V_t is the thermal voltage (26 mV at 300 K) and η is the sub-threshold swing parameter. We note that I_{ds} increases exponentially with a decrease in V_T . This is why a reduction in supply voltage (which is accompanied by a reduction in threshold voltage) results in exponential increase in leakage.

Another observation that can be made from (1) is that I_{ds} is significantly larger when $V_{ds}>>\eta V_t$. For typical devices, this is satisfied when $V_{ds}\sim V_{DD}$. The reason for this is not only that the last term of (1) is close to unity, but also that with a large value of $V_{DS}.V_T$ would be lowered due to drain induced barrier lowering (DIBL) V_T decreases approximately linearly with increasing V_{ds} [3], [2]. Therefore, leakage reduction techniques should ensure that the supply voltage is not applied across a single device, as far as possible.

In recent times, leakage power reduction has received much attention in academic research as well as industrial applications. Several means of reducing leakage power have been proposed. In [8], the authors propose a dynamic threshold MOSFET design for low leakage applications. In this scheme, the device gate is connected to the bulk, resulting in high-speed switching and low leakage currents through body effect control. The drawback of this approach is that it is only applicable in situations where is lower than the diode turn-on voltage. Also, the increased capacitance of the gate signal slows the device down, and as a result, the authors propose the use of this technique for partially depleted silicon on insulator (SOI) designs. Another methodology for controlling leakage is the variable threshold (often called VTCMOS) approach.

In such an approach, the device threshold voltages are controlled dynamically by modifying the device bulk voltage. This method offers the advantage of decreasing the leakage in standby mode while not increasing the delay in the active mode.. However, complex control circuitry is required to generate and control the bulk voltages. Another drawback is that the bulk terminals have to be electrically isolated from the source terminals of the devices and this may require some major changes in cell layout. In another approach called the super cut-off CMOS (SCCMOS) approach, the gate of a PMOS device which gates the V_{DD} supply is overdriven, thereby reducing the leakage dramatically. This again requires the design of complex circuitry to generate and control the special over-driven voltage values.

II. MULT-THRESHOLD CMOS

The concept of Multi- Threshold CMOS (MTCMOS) which has emerged as a very popular technique for standby mode leakage power reduction.

In this technique, a high-threshold voltage transistor is inserted in series with the power supply and the existing design and ground as shown in Figure**.** The working of this circuit is as follows. During Active mode of operation, the high threshold Vt transistors are turned on, thereby facilitating normal operation of the circuit as there exists a direct

path from the output to ground and Vdd. During Standby mode, these transistors are turned off creating a virtual power supply and ground rail and cutting off the circuit from supply.

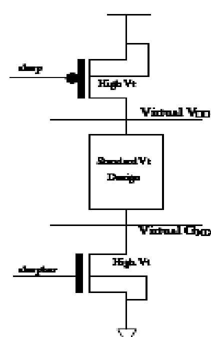


Fig. 2.1 MTCMOS Structure

Since the high Vt transistors operating in standby mode forces the circuit to go to"sleep", they are also known as sleep transistors. Thus, in this technique both standard – and high - threshold voltages are fabricated on a single chip. From a visual perspective, these high Vt sleep transistors act as a current gate to the designed circuit. For this reason, this technique is also referred to as Power Gating.

Effect of Introducing Sleep Transistors in Active Mode

Consider the Pull Up Network (PUN) of a static CMOS circuit. A PMOS sleep transistor is inserted between V_{dd} source and the PUN. During the normal mode of circuit operation, the sleep transistors can be modeled as a resistor R as shown in Figure. Assuming that the current flowing into the transistor is I, this resistance will cause a voltage drop across it, say V_{sleep}. Therefore, the gate driving capability reduces to $V_{dd} - V_{sleep}$ from V_{dd}. This reduction in driving capability causes degradation in circuit performance.

To overcome this problem, it is essential to lower the resistance R of the transistor as much as possible. This in turn implies increasing the size (width) of the the transistor, since the resistance of the transistor is inversely proportional to its width. This, however, comes at an expense of increased area and dynamic power dissipation. Conversely, a small size transistor would degrade the circuit speed. A solution to this problem would be to reduce the threshold voltage Vt but as seen from Equation 1, the sub-threshold current and hence the leakage power would increase exponentially. Hence, there is a clear trade-off between area, power and delay metrics of a circuit for low leakage designs.

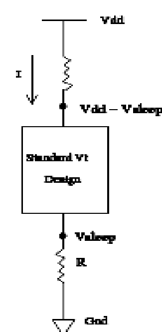


Figure 2.2 Sleep Transistor modeled as Resistor

III. PROPOSED METHOD

This paper deals with low-leakage ASIC design using specialized standard cells. Based on the discussion of the previous section, we know that I_{ds} would be significantly larger When $Vds >> \eta V_t$. This is because V_T drops due to DIBL when V_{ds} is Large. This causes the first term of (1) to increase exponentially, while the parenthesized term of (1) is close to 1. Our approach to leakage reduction attempts to ensure that the supply voltage is applied across more than one turned-off device and one of those devices is a high-V_T device. This is achieved by selectively introducing a high- V_T PMOS or NMOS supply gating device. By this design choice, we obtain standard cells with both low and predictable standby leakage currents. Our goal is to design standard cells with predictably low leakage currents. To achieve this purpose, we design two variants of each standard cell. The two variants of each standard cell are designated "H" and "L." If the inputs of a cell during the standby mode of operation are such that the output has a high value, we minimize the leakage in the pull-down network. So a footer device (a high-V_T NMOS with its gate connected to standby) is used. We call such a cell the "H" variant of the standard cell. Similarly, if the inputs of a cell during the standby mode of operation are such that the output has a low value, we minimize the leakage in the pull-up network by adding a header device (a high- V_T PMOS with its gate connected standby), and call such a cell the "L" variant of the standard cell. This exercise, when carried out for a NAND3 gate, yields Circuits shown in Fig. 1.Note that the MTCMOS circuit is also shown here. Although the PMOS and NMOS supply gating devices (equivalently called header and footer devices (devices shown shaded in Fig. 1) are shown in the circuit for the MTCMOS design, such devices are in practice shared by all the standard cells of a larger circuit block.

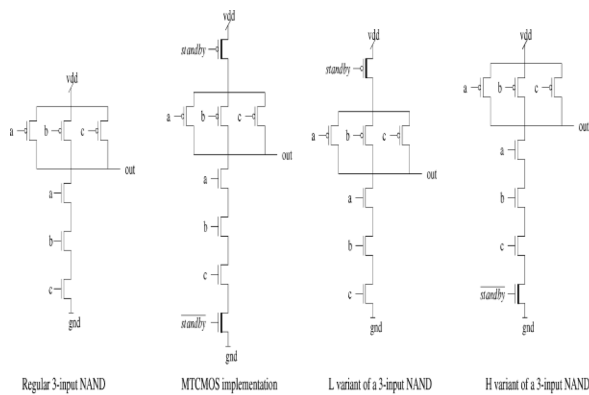


Fig. 3.1 Transistor Level Description

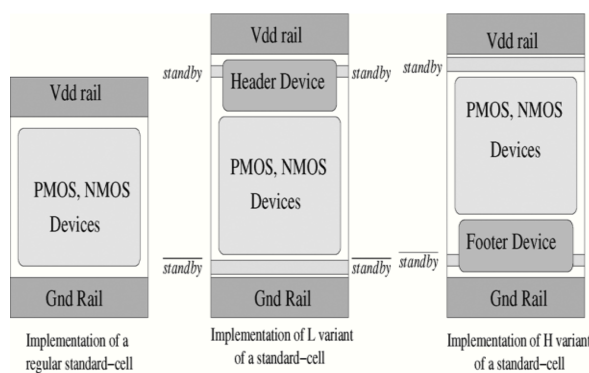


Fig. 3.2. Layout flop-plan of HL-gates

We sized the header and footer devices so that the worst-case output delay penalty over all gate input transitions was no larger than 15% as compared to the regular standard cell using low transistors

IV. SIMULATION RESULTS

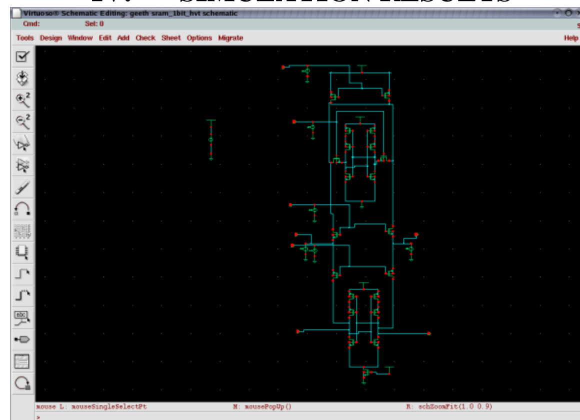


Fig .4.1 High-V_t SRAM cell

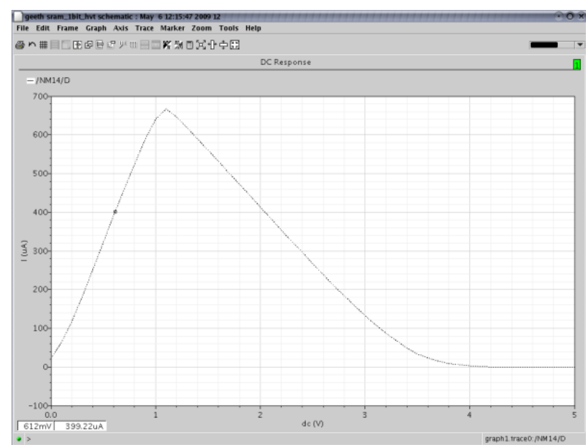


Fig .4.2 D.C Response of High-V_t SRAM cell

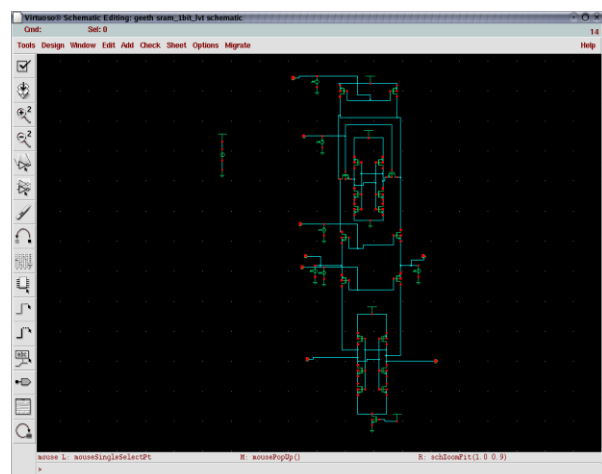


Fig. 4.3 Low-V_t SRAM Cell

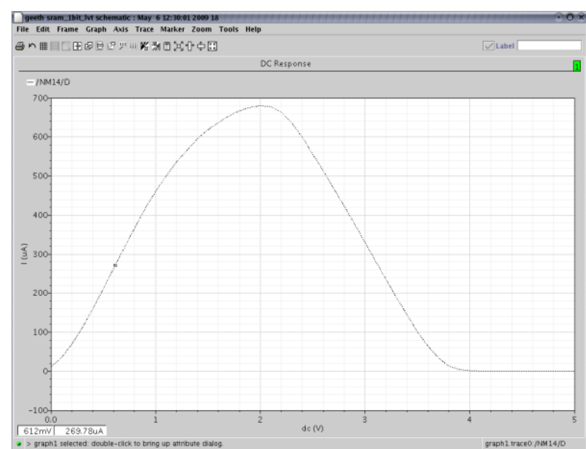
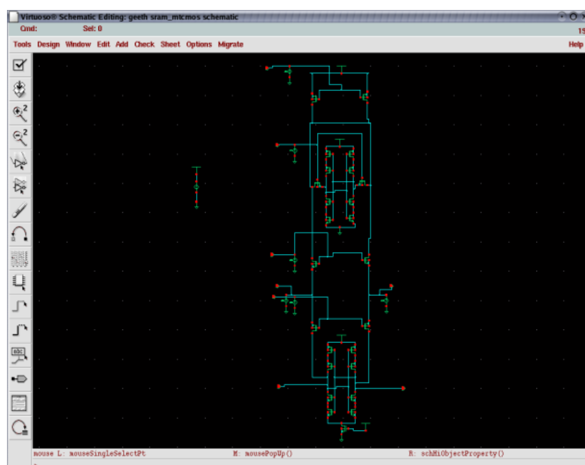


Fig. 4.4 D.C Response of Low-V_t SRAM cell



eFig. 4.5 MTCMOS SRAM Cell

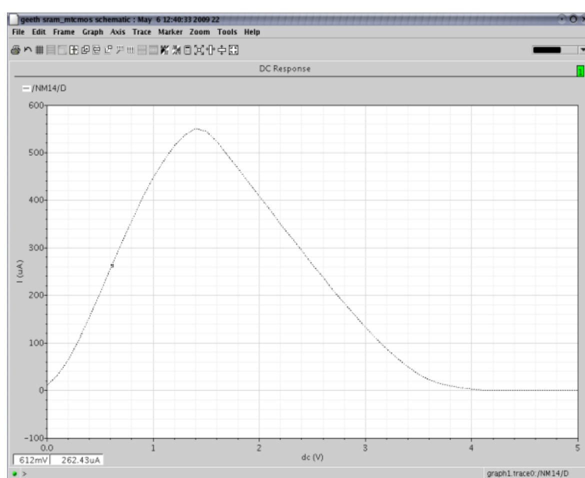


Fig.4.6 D.C Response of SRAM Cell

V. CONCLUSION

In this paper, we have explored low-leakage standard cell based ASIC design methodologies for SRAM cell. We implemented low leakage SRAM cell for different cases such as high-V_t, low-V_t and MTCMOS methodology. By out technique we can reduce the leakage currents to nearly 50-60% thereby operating the cell at low power.

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